CPU64 - technical document, webpage: http://www.ide64.org

CPU FPGA instructions - draft

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	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	BRK s	ORA (zp,X)				ORA zp	ASL zp	ASL l	PHP s	ORA #	ASL A			ORA a	ASL a	ORA l
1	BPL r	ORA (zp),Y		ORA l,Y		ORA zp,X	ASL zp,X	ASL l,X	CLC i	ORA a,Y	INC A			ORA a,X	ASL a,X	ORA l,X
2	JSR a	AND (zp,X)	JSR l		BIT zp	AND zp	ROL zp	ROL l	PLP s	AND #	ROL A		BIT a	AND a	ROL a	AND l
3	BMI r	AND (zp),Y		AND l,Y	BIT zp,X	AND zp,X	ROL zp,X	ROL l,X	SEC i	AND a,Y	DEC A		BIT a,X	AND a,X	ROL a,X	AND l,X
4	RTI s	EOR (zp,X)				EOR zp	LSR zp	LSR l	PHA s	EOR #	LSR A		JMP a	EOR a	LSR a	EOR l
5	BVC r	EOR (zp),Y		EOR l,Y		EOR zp,X	LSR zp,X	LSR l,X	CLI i	EOR a,Y	PHY s		JMP l	EOR a,X	LSR a,X	EOR l,X
6	RTS s	ADC (zp,X)				ADC zp	ROR zp	ROR l	PLA s	ADC #	ROR A	RTL s	JMP (a)	ADC a	ROR a	ADC l
7	BVS r	ADC (zp),Y		ADC l,Y		ADC zp,X	ROR zp,X	ROR l,X	SEI i	ADC a,Y	PLY s			ADC a,X	ROR a,X	ADC l,X
8	BRA r	STA (zp,X)		STY l	STY zp	STA zp	STX zp	STX l	DEY i	BIT #	TXA i	PHB s	STY a	STA a	STX a	STA l
9	BCC r	STA (zp),Y		STA l,Y	STY zp,X	STA zp,X	STX zp,Y	STX l,Y	TYA i	STA a,Y	TXS i		STZ a	STA a,X	STZ a,X	STA l,X
A	LDY #	LDA (zp,X)	LDX #	LDY l	LDY zp	LDA zp	LDX zp	LDX l	TAY i	LDA #	TAX i	PLB s	LDY a	LDA a	LDX a	LDA l
B	BCS r	LDA (zp),Y		LDA l,Y	LDY zp,X	LDA zp,X	LDX zp,Y	LDX l,Y	CLV i	LDA a,Y	TSX i		LDY a,X	LDA a,X	LDX a,Y	LDA l,X
C	CPY #	CMP (zp,X)			CPY zp	CMP zp	DEC zp	DEC l	INY i	CMP #	DEX i		CPY a	CMP a	DEC a	CMP l
D	BNE r	CMP (zp),Y		CMP l,Y		CMP zp,X	DEC zp,X	DEC l,X	CLD i	CMP a,Y	PHX s			CMP a,X	DEC a,X	CMP l,X
E	CPX #	SBC (zp,X)			CPX zp	SBC zp	INC zp	INC l	INX i	SBC #	NOP i		CPX a	SBC a	INC a	SBC l
F	BEQ r	SBC (zp),Y				SBC zp,X	INC zp,X	INC l,X	SED i	SBC a,Y	PLX s			SBC a,X	INC a,X	SBC l,X

CPU 6510
CPU FPGA
CPU 65816
CPU 65C02